IN THE CLAIMS

~~Current status of the claims:~~

Claims 1-18 (Canceled).

19. (Previously Amended) A method of making an integrated circuit, comprising the step of plating a conductive material to project outwardly from a second surface of a substrate to form a lead-free first lead of the integrated circuit.

20. (Previously Amended) The method of claim 19, further comprising the step of mounting a semiconductor die to a first surface of the substrate.

21. (Previously Amended) The method of claim 20, further comprising the step of forming a signal path on the first surface with the conductive material.

22. (Previously Amended) The method of claim 21, further comprising the step of disposing the conductive material in a via defined by the substrate to extend the signal path from the first surface to the second surface of the substrate.

23. (Previously Amended) The method of claim 22, further comprising the step of disposing the conductive material on the second surface to extend the signal path from the via to the lead-free first lead.

24. (Previously Amended) The method of claim 23, wherein the step of disposing the conductive material on the second surface includes the step of forming an access pad on the second surface.

25. (Previously Amended) The method of claim 23, further comprising the steps of:

disposing a photoresist layer on the second surface;

patterning the photoresist layer to expose the access pads; and

plating the conductive material on the access pads.

26. (Original) The method of claim 25, wherein the step of patterning includes the step of forming an opening in the photoresist layer over the access pads.

27. (Original) The method of claim 26, wherein the step of plating includes the step of plating the conductive material within the opening.

28. (Previously Amended) The method of claim 21, further comprising the step of wire bonding the signal path to a node of the semiconductor die to couple a signal between the node and the lead-free first lead.

29. (Previously Amended) The method of step 19, further comprising the step of forming a solder mask on the second surface between the lead-free first lead and a lead-free second lead of the integrated circuit.

30. (Original) The method of claim 29, wherein the step of forming includes the step of forming the solder mask after the step of plating.

31. (Previously Amended) The method of claim 19, wherein the step of plating includes the step of plating the conductive material in an outward direction for routing a current (I_{SIGNAL}) through the lead-free first lead that flows parallel to the outward direction.

32. (Previously Amended) A method of forming an integrated circuit, comprising the steps of:

providing a substrate having a first surface for mounting a semiconductor die; and

plating a conductive material to extend outwardly from a second surface of the substrate to form a lead-free lead of the integrated circuit.

33. (Original) The method of claim 32, wherein the step of plating includes the step of disposing the conductive material to a height for attaching the lead to a mounting surface.

34. (Original) The method of claim 33, wherein the step of disposing includes the step of disposing the conductive material to the height of at least fifty micrometers.

35. (Original) The method of claim 33, wherein the step of disposing includes the step of forming the lead to a height that maintains a spacing between the substrate and the motherboard.